

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 7,167,032 B1  
APPLICATION NO. : 10/815403  
DATED : January 23, 2007  
INVENTOR(S) : Danny S. Barlow

Page 1 of 5

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

The Title page, showing an illustrative figure, should be deleted and substitute therefor the attached title page.

Delete 3 Formal Drawing sheets 1, 3 and 4, for Figure 1, Figure 3A, and Figure 3B and substitute therefor the Drawing sheets, consisting of figs. 1, 3A-3B as shown on the attached pages.

Signed and Sealed this

Twenty-second Day of September, 2009

A handwritten signature in black ink that reads "David J. Kappos". The signature is written in a cursive, flowing style with a large initial 'D' and a stylized 'K'.

David J. Kappos  
*Director of the United States Patent and Trademark Office*

(12) **United States Patent**  
**Barlow**

(10) **Patent No.:** **US 7,167,032 B1**  
(45) **Date of Patent:** **Jan. 23, 2007**

(54) **SELF-ADJUSTING SCHMITT TRIGGER**

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(\*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(h) by 0 days.

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**H03K 3/12** (2006.01)

(52) **U.S. Cl.** ..... 327/205

(58) **Field of Classification Search** ..... 327/205,  
327/206, 208, 210  
See application file for complete search history.

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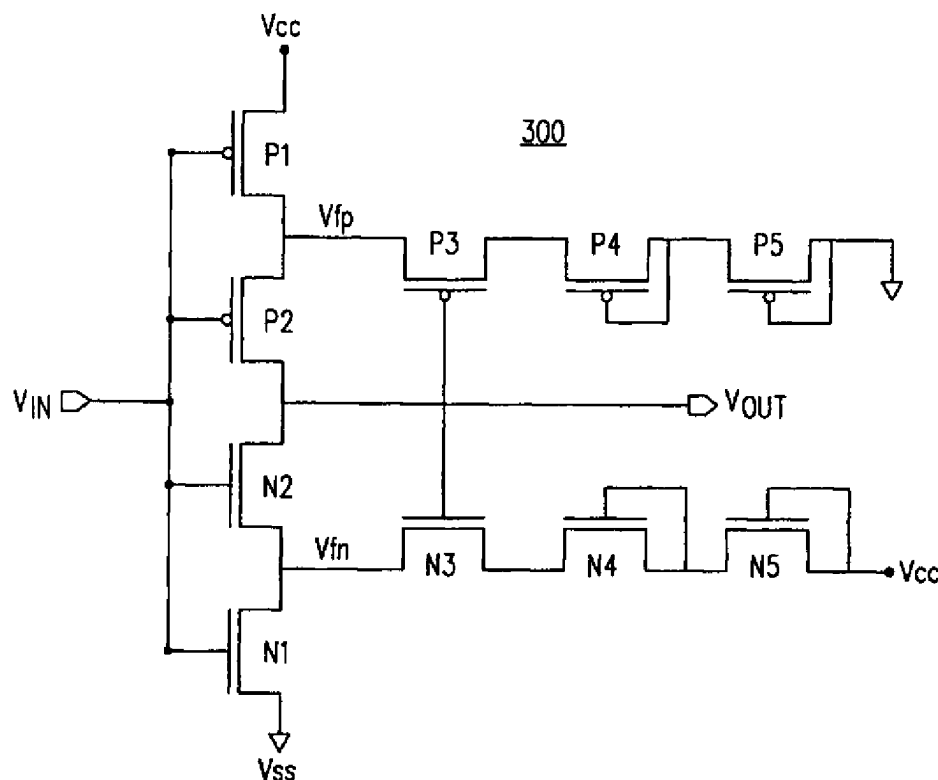
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(57) **ABSTRACT**

A Schmitt trigger includes a PMOS transistor and an NMOS transistor, each having a gate coupled to an output voltage terminal. The Schmitt trigger is configured such that an input voltage that switches on the PMOS transistor determines a low voltage threshold and an input voltage that switches on the NMOS transistor determines a high voltage threshold. By coupling devices such as diodes to either or both of the PMOS and NMOS transistors, a margin between the low voltage threshold and ground and between the high voltage threshold and a supply voltage are maintained as the supply voltage is reduced. In addition, hysteresis is maintained or increased as supply voltage is increased.

**19 Claims, 5 Drawing Sheets**



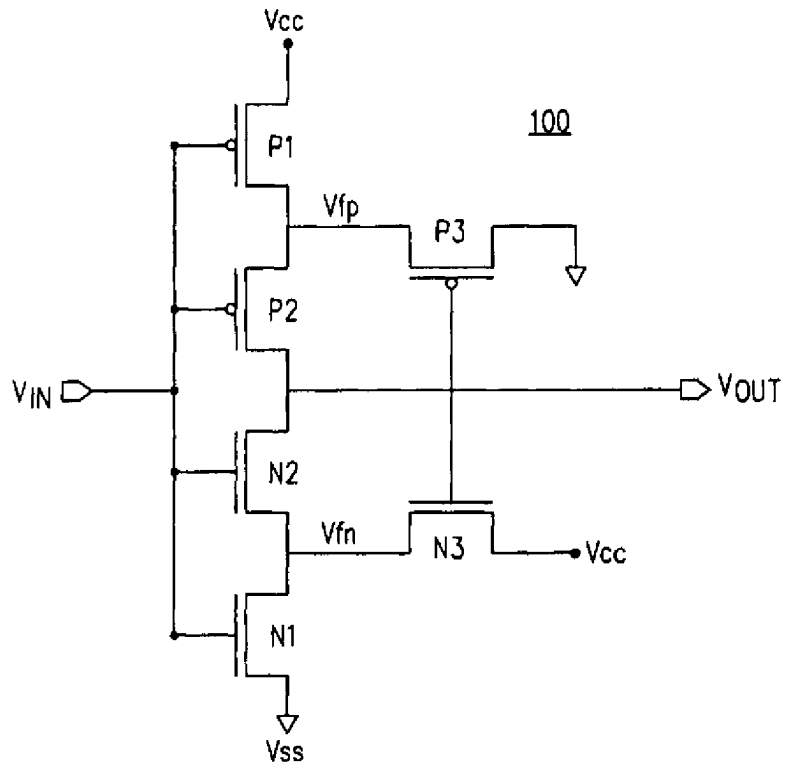


FIG. 1  
(PRIOR ART)

